#### On Symmetric Circuits and FPC

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# **Context / Motivation**

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Characterises first-order logic FO by uniform constant-depth poly-size symmetric Boolean circuits.

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#### Theorem

P-uniform poly-size symmetric threshold circuits = FPC.

Vocabulary au

#### Finite $\tau$ -structures fin $[\tau]$

**FPC** Inflationary fixed-point logic extended with the ability to express the size of definable sets.

- Assume standard syntax and semantics.
- Expresses properties invariant to isomorphisms of structures.

### **Colored DAGs**

- A  $\mathbb{C}$ -Colored Directed Acyclic Graph (CDAG) over a set U:
  - Gates G
  - Inputs I
  - Directed edges E form acyclic graph on  $G \uplus I$  with leaves I with a single root gate r.
  - Coloring  $\xi: G \uplus I \to \mathbb{C}$
  - Input Tuples  $\lambda: I \to U^k$





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Each node in a circuit naturally evaluates to a Boolean value.

• A circuit is invariant if the value computed at the root is independent of isomorphisms of the structure.

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- A family of invariant Boolean circuits on τ-structures for all sizes of U defines a function fin[τ] → {0,1}.

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- takes  $i \in I$  to  $\pi(i) \in I$  with

**1**  $\xi(i) = \xi(\pi(i))$ , and **2**  $\pi(\lambda(i)) = \pi(u_1, \dots, u_k) := (\sigma(u_1), \dots, \sigma(u_k)) = \lambda(\pi(i))$ ; and

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Call C symmetric if  $\forall \sigma \in \operatorname{Sym}_U$ ,  $\sigma$  induces an automorphism of C.



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- Define Supp(C) to be the maximum over all nodes v of the number of elements in all but the largest part of Supp(v).

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# **Support Theorem**

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#### Support Theorem

For any  $1 > \epsilon \ge \frac{2}{3}$ , let C be a symmetric s-node CDAG over U with  $\log |U| \ge \frac{56}{\epsilon^2}$ , and  $s \le 2^{|U|^{1-\epsilon}}$ . Then  $\operatorname{Supp}(C) \le \frac{33}{\epsilon} \frac{\log s}{\log |U|}$ . Supp(C) is tightly constrained by the number of nodes in C.

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#### Corollary

Poly-size symmetric CDAGs have constant support.

# Application: symmetric threshold circuits = FPC

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#### Proof Idea

- Generate the P-uniform circuit over the number sort, using the Immerman-Vardi theorem.
- 2 Label gates with their support partition.
- 3 Transform labels into tuples by duplicating gates.
- 4 Determine equality test indicating edges.
- 5 Evaluate circuit w.r.t. unordered universe using equality test.

Consider arithmetic circuits whose inputs are matrices  $X \in \mathbb{F}^{U \times U}$ :

- Constants 0, and 1.
- Basis  $+, -, and \times$ .
- Variables  $X = \{x_{u,v}\}_{u,v \in U}$ .

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Context:  $2^{\Omega(\log^2 |U|)}$  size for multilinear formulas [Raz '08].



#### Support Theorem

For any  $1 > \epsilon \ge \frac{2}{3}$ , let C be a symmetric s-node CDAG over U with  $\log |U| \ge \frac{48}{\epsilon}$ , and  $s \le 2^{|U|^{1-\epsilon}}$ . Then  $\operatorname{Supp}(C) \le \frac{24}{\epsilon} \frac{\log s}{\log |U|}.$ 

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Applications:

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# **Open Questions**

- Can the notion of support be generalised:
  - to multi-sorted domains,
  - to subgroups of  $\operatorname{Sym}_U$ , or
  - to larger ranges of  $\epsilon$ ?
- Are there other applications in logic or circuit complexity?
- Is there a similar circuit characterisation of CPT(Card)?

# Thanks!